CLAIMS

1. A semiconductor chip comprising:

a common circuit block which is operative at a first voltage and a second voltage that is higher than the first voltage;

a first circuit block which is designed to fit the first voltage and operate in unison with said common circuit block;

a second circuit block which is designed to fit the second voltage and operate in unison with said common circuit block; and

a voltage type setup circuit which activates one of said first and second circuit blocks,

wherein said semiconductor chip holds a first identification record indicative of the operability at the first voltage or a second identification record indicative of the operability only at the second voltage.

2. A semiconductor chip according to claim 1,

wherein said common circuit block is operative at a third voltage that is higher than the second voltage,

wherein said semiconductor chip further includes a third circuit block which is designed to fit the third voltage and operate in unison with said common circuit block,

wherein said voltage type setup circuit activates one of said first, second and third circuit blocks, and

wherein the first and second identification records

correspond to the operability at the first and second voltages, respectively, and said semiconductor chip further holds a third identification record indicative of the operability only at the third voltage.

3. A semiconductor chip according to claim 2, wherein the first, second and third identification records are memorized in an electrically writable nonvolatile memory means.

4. A semiconductor chip according to claim 2,

wherein the first identification record indicates inclusively the operability also at the second and third voltages, and

wherein the second identification record indicates inclusively the operability also at the third voltage.

5. A semiconductor chip according to claim 2, wherein said voltage type setup circuit selects one of said first, second and third circuit blocks based on the combination of a bonding pad which is given the ground voltage or power voltage during the bonding process and an electrically writable memory means.

6. A semiconductor integrated circuit device using a semiconductor chip, the chip comprising:

a common circuit block which is operative at a first voltage

and a second voltage that is higher than the first voltage;

a first circuit block which is designed to fit the first voltage and operate in unison with said common circuit block;

a second circuit block which is designed to fit the second voltage and operate in unison with said common circuit block; and

a voltage type setup circuit which activates one of said first and second circuit blocks,

said voltage type setup circuit selecting one of said first and second circuit blocks if said semiconductor chip is operative at the first voltage or selecting said second circuit block if said semiconductor chip is operative only at the second voltage.

7. A semiconductor integrated circuit device according to claim 6,

wherein said common circuit block is operative at a third voltage that is higher than the second voltage,

wherein said semiconductor chip further includes a third circuit block which is designed to fit the third voltage and operate in unison with said common circuit block,

wherein said voltage type setup circuit activates one of said first, second and third circuit blocks, and

wherein said voltage type setup circuit selects one of said first, second and third circuit blocks if said semiconductor chip is operative at the first voltage, selects one of said second

and third circuit blocks if said semiconductor chip is operative at the second voltage, or selects said third circuit block if said semiconductor chip is operative only at the third voltage.

8. A semiconductor integrated circuit device according to claim 7, wherein said voltage type setup circuit selects one of said first, second and third circuit blocks based on the combination of a bonding pad which is given the ground voltage or power voltage during the bonding process and an electrically writable memory means.

9. A semiconductor integrated circuit device according to claim 8, wherein each of said first, second and third circuit blocks includes, as circuit blocks of a flash memory, a sense amplifier which reads out stored data of nonvolatile memory cells, a charge pump circuit which produces voltages for the write and erase operations, an oscillation circuit, a power-on detection circuit, a voltage fall detection circuit, and an output buffer which releases the read-out data.

10. A semiconductor integrated circuit device according to claim 9, wherein said charge pump circuit comprises a multi-stage charge pump circuit which is designed to fit the first voltage, with the number of stages counted from the output stage being switched by the selection signals corresponding to the

second and third voltages provided by said voltage type setup circuit.

11. A semiconductor integrated circuit device according to claim 9, wherein said bonding pad is used to specify the first, second or third voltage and said electrically writable memory means is used to specify the second or third voltage.

12. A semiconductor integrated circuit device according to claim 11, wherein said bonding pad is connected to an external terminal.

13. A semiconductor integrated circuit device according to claim 12, wherein said first, second and third voltages are 1.8 V,2.5 V and 3.0 V, respectively.

14. A method of manufacturing semiconductor integrated circuit devices each based on a semiconductor chip which comprises:

a common circuit block which is operative at a first voltage and a second voltage that is higher than the first voltage;

a first circuit block which is designed to fit the first voltage and operate in unison with said common circuit block;

a second circuit block which is designed to fit the second voltage and operate in unison with said common circuit block;

and

a voltage type setup circuit which activates one of said first and second circuit blocks,

said method implementing, commonly for all semiconductor chips, a front-end process including the formation of said semiconductor chips on a wafer up to a probing process for testing the operability of said semiconductor chips on said wafer at the first and second voltages,

implementing a first assembly process including the setup of the first voltage to said voltage type setup circuit for a chip which has been proved to be operative at the first voltage in accordance with the test result and the demand of products, and

implementing a second assembly process including the setup of the second voltage to said voltage type setup circuit for a chip which has been proved to be operative at the first voltage and for a chip which has been proved to be operative only at the second voltage in accordance with the test result and the demand of products.

15. A method of manufacturing semiconductor integrated circuit devices according to claim 14,

wherein said common circuit block is operative at a third voltage that is higher than the second voltage,

wherein said semiconductor chip further includes a third

circuit block which is designed to fit the third voltage and operate in unison with said common circuit block, and said voltage type setup circuit activates one of said first, second and third circuit blocks,

wherein said probing test further tests the operability of said semiconductor chips on said wafer at a third voltage,

wherein said first assembly process sets the first voltage to said voltage type setup circuit for a chip which has been proved to be operative at the first voltage,

wherein said second assembly process sets the second voltage to said voltage type setup circuit for a chip which has been proved to be operative at the first and second voltages, and

wherein said method further includes a third assembly process including the setup of the third voltage to said voltage type setup circuit for a chip which has been proved to be operative at the first and second voltages and for a chip which has been proved to be operative only at the third voltage.

16. A method of manufacturing semiconductor integrated circuit devices according to claim 15,

wherein said probing process tests the operability of said semiconductor chips on said wafer at the first, second and third voltages, and determines a chip, which has failed the tests at all voltages, to be defective.

17. A method of manufacturing semiconductor integrated circuit devices according to claim 16,

wherein the setup of voltage type is implemented by the application of the ground voltage or power voltage to the voltage setup bonding pad of the bonding process during the first, second and third assembly processes.

18. A method of manufacturing semiconductor integrated circuit devices according to claim 17,

wherein said semiconductor integrated circuit device is rendered the marking on the package thereof in correspondence to the set-up voltage type during the first, second and third assembly processes.

19. A memory apparatus comprising:

a first memory chip;

a second memory chip; and

a designated terminal to be supplied an operation voltage,

wherein said first memory chip has a first terminal, a second terminal and a voltage circuit,

wherein said second memory chip has a third terminal,

wherein said designated terminal couples to said first terminal of said first memory chip and said third terminal of said second memory chip and is supplied an operation voltage,

wherein said second terminal of said first memory chip is

supplied one of a first state signal and a second state signal according to a voltage level of said operation voltage,

wherein said second terminal is supplied said first state signal, said first memory chip is supplied a first voltage as said operation voltage and generates an internal operation voltage from said first voltage by said voltage circuit,

wherein said second terminal is supplied said second state signal, said first memory chip is supplied a second voltage as said operation voltage and generates said internal operation voltage from said second voltage by said voltage circuit, and

wherein said first voltage is lower voltage than said second voltage.

20. A memory apparatus according to claim 19,

wherein said voltage circuit comprises a charge pump including a plurality of stages,

wherein when said second terminal is supplied said first state signal, said voltage circuit uses a first stage of said charge pump,

wherein when said second terminal is supplied said second state signal, said voltage circuit uses a second stage of said charge pump, and

wherein a boost rate of said first stage is more than a boost rate of said second stage.

21. A memory apparatus according to claim 20, further comprising a fourth terminal,

wherein said fourth terminal is supplied a reference voltage,

wherein said second terminal is fixedly coupled to one of said operation voltage or said reference voltage as said first state signal, and

wherein said second terminal is fixedly coupled to another one of said operation voltage or said reference voltage as said second state signal.

22. A memory apparatus according to claim 21,

wherein said reference voltage is a ground level.

23. A memory apparatus according to claim 22,

wherein said first memory chip is a volatile memory, and

wherein said second memory chip is a nonvolatile memory.

24. A nonvolatile memory apparatus comprising:

a first semiconductor chip;

a nonvolatile memory chip; and

a designated terminal pair for being supplied an operation voltage,

wherein said first semiconductor chip has a first terminal pair coupled to said designated terminal pair,

wherein said nonvolatile memory chip has a voltage circuit, a second terminal pair coupled to said designated terminal pair and a third terminal for being supplied one of a first state signal and a second state signal according to a voltage level of said operation voltage,

wherein when said third terminal is supplied said first state signal, said nonvolatile memory chip is supplied a first voltage as said operation voltage and generates an internal operation voltage from said first voltage by said voltage circuit,

wherein when said third terminal is supplied said second state signal, said nonvolatile memory chip is supplied a second voltage as said operation voltage and generates said internal operation voltage from said second voltage by said voltage circuit and,

wherein said first voltage is lower than said second voltage.

25. A nonvolatile memory apparatus according to claim 24,

wherein said nonvolatile memory has a nonvolatile memory array, wherein said voltage circuit generates a program voltage for programming data to said nonvolatile memory array.

26. A nonvolatile memory apparatus according to claim 25,

wherein said voltage circuit further generates an erase voltage for erasing data stored in said nonvolatile memory array.

27. A nonvolatile memory apparatus according to claim 26, wherein when said first semiconductor chip is only operable by said second voltage as said operation voltage, said third terminal of said nonvolatile memory is fixedly supplied said second state signal.